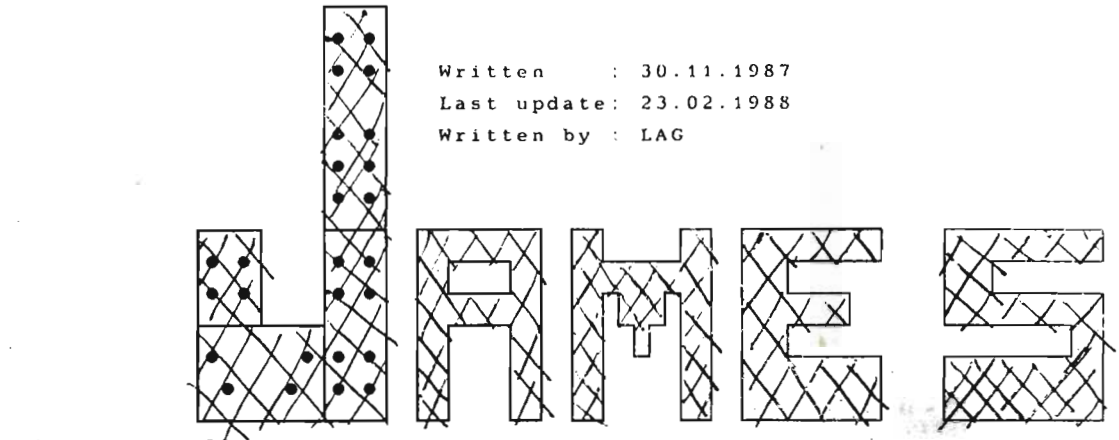


Written : 30.11.1987
Last update: 23.02.1988
Written by : LAG

MFbus controller
POrt controller
Domino
Ethernet controller

```
HH  HH AAAAAA RRRRRR DDDDD  WW    WW AAAAAA RRRRRR EEEEEE
HH  HH AA  AA RR  RR DD  DD WW    WW AA  AA RR  RR EE
HHHHHH AAAAAA RRRRRR DD  DD WW WW WW AAAAAA RRRRRR EEEE
HH  HH AA  AA RR RR  DD  DD WW WW WW AA  AA RR RR  EE
HH  HH AA  AA RR  RR DDDDD   WWWWW  AA  AA RR  RR EEEEEE

DDDDD  EEEEEE SSSSSS CCCCCC RRRRRR III PPPPPP TTTTTT III OOOOOO NN  NN
DD  DD EE     SS     CC     RR  RR III PP  PP   TT   III OO  OO NNNNNN
DD  DD EEEE   SSSSSS CC     RRRRRR III PPPPPP   TT   III OO  OO NN NNN
DD  DD EE         SS CC     RR RR  III PP       TT   III OO  OO NN NNN
DDDDD  EEEEEE SSSSSS CCCCCC RR  RR III PP       TT   III OOOOOO NN  NN
```

1. Intoduction.

This paper describes the print M5471A1. The main functions in the print is:

- MFbus controller.
- ND100 port.
- Domino Ethernet controller.

The functions of the MFbus controller part is a superset of the existing MFbus controller functions.
The functions of the ND100 port is nearly the same as on the Double Bus controller.
The functions of Ethernet controller is exactly the same as Domino Ethernet III.

1.1 Notation in the text.

The signals described in the text may have two different levels:

$INTL_0$ is active low, active if "0" ("$_0$" means active low).
PTOTR is active high, active if "1".

All addresses are hexadecimal.

2. Address decoding.

The address space is devided into three parts:

- Std. Domino address space
- MFbus interface address space
- Ethernet interface address space

The two last parts are described in the belonging chapters below. For the Std. Domino it is refered to the Domino description.

3. Standard Domino part.

See the "Domino hardware description" manual.

4. MFbus part.

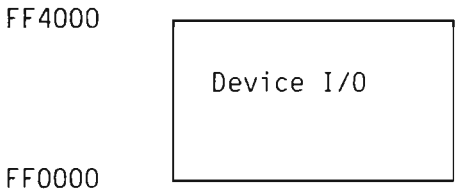
4.1 MFbus interface address decoding.

The additional registers are due to the MFbus control function of James. The registers are:

- MFbus-part control register MFCR
- Error logs
- MFbus-part status register MFSR
- Master to the loadmeter
- The contents of the loadmeter
- Clear the loadmeter
- Global time-out register
- Local time-out register
- ND100 base address register
- The second consoll

Also one EEPROM (in the backwiring) and a SRAM with clock is defined in the MFbus part.

The MFbus part registers, Ethernet registers, EEPROM and SRAM are accessed as Device I/O (see Domino manual). This is pointed out as $IOSEL_0$.



The addres decoding is as follows:

FF0000 - FF0046	Ethernet*	(16 bit)
FF1000	Read/write MFpart controll register MFCR	(32 bit)
FF1004	Read MFpart status register MFSR	(32 bit)
FF1008	Clear loadmeter	(32 bit)
FF1008	Read loadmeter	(32 bit)
FF100C	Write master to loadmeter	(32 bit)
FF1010	Write local MFbus time-out	(32 bit)
FF1014	Write global MFbus time-out	(32 bit)
FF1020		
FF1024	Read error-logs interrupt from error-log	(32 bit)
FF1028		
FF102C		
FF1030	Write base address for ND100 port	(32 bit)
FF1040 - FF105F	Write/read to the second consoll	(32 bit)
FF1800 - FF1FFF	Read/write the SRAM	(8 bit)
FF2000 - FF27FF	Read/write the EEPROM in the backwiring	(8 bit)
(FF2000 - FF3FFF) if 8k byte EEPROM		

Note * : Futher description of the address decoding of Ethernet registers are given in chapter "Ethernet".

4.2 Additional registers inside MFbus part.

4.2.1 The MFbus-part control register MFCR.

The control register is including:

data signal	signal name	
MD31	AR31	Keep clear of this bit until it is futher decided what the function is going to be.
MD30	DISNAVAL	Disable the $BNAVAL_0$ signal on the MFbus (not used when read).
MD29	PCST	Programmable COLD-START.
MD28	PWST	Programmable WARM-START.
MD27	ROT_0	Rotational priority of the MFbus.
MD26	PTOTR	Prgrammable $BTOTRES_0$.
MD25		NOT USED
MD24	REW	
MD23	$LOGALL_0$	Log the contents of the MFbus.
MD22	$COUNTALL_0$	When active the loadmeter counts all MFbus data cycles. If inacitve it counts only the cycles that belongs to one certain master.
MD21	COUNTEN	Enable the counter.
MD20	TESTCOUNT	The counter is tested with a 16MHz clock.
MD19	ENTWOC	Enable the watch-dog for direct reset.
MD18	BVPP	Programming pulse to the external EEPROMs

MD17

MD16

4.2.2 The MFbus-part status register MFSR.

The following signals are availible:

MD31	LMETOVF	Loadmeter has an overflow. The content is not realible.
MD30	$INTL_0$	Interrupt from the error-log part.
MD29	SPEED1	Octobus speed.
MD28	SPEED0	Octobus speed.
MD27	TIMEOUT	The controller has had an internal time-out
MD26	MFTIMINT	MFbus has a critical time-out that is not repaired.
MD25	SLOT4	Slot code bit 4.
MD24	SLOT3	Slot code bit 3.
MD23	SLOT2	Slot code bit 2.
MD22	SLOT1	Slot code bit 1.
MD21	SLOT0	Slot code bit 0.

4.2.3 The loadmeter.

The loadmeter is counting all or some data cycles on the MFbus (see $COUNTALL_0$ above). If it is counting only data cycles belonging to one master, the master code must be written into a register:

MD31 MD27

master code

The contents of the loadmeter is read into MD(31:16). Bit 31 in MFSR indicates an overflow.

The loadmeter is cleared by writing to it.

4.2.4 The time-out registers.

There are two time-out registers for the MFbus, one for local- and one for global time-out. The maximum time-out is 61usec for both. The resolution is 240nsec. The format is:

OFF1010H

MD07	MD00
time-out-value	

The time-out is then : time-out-value * 240nsec.

Timeout for ~~BUS~~ BARA-om

OFF ~~nloolig~~

~~OFF~~ ~~65 µsec.~~

0F	60 µsec.
00	64 µsec.
20	56 µsec
~~70~~	36 µsec.
A0	24 µsec
C1	16 µsec.
E0	83 µsec
E1	8,0
~~E0~~	4,3 µsec
~~EF~~	
FA	1,8 µsec
FB	1,76 µsec ± 0,1
FE	945 nsec
FF	930

4.2.5 Error-logs.

There are three error-logs:

FF1020	Read error log 1
FF1024	Read error log 2
FF1028	Read error log 3
FF102C	Clear interrupt from error log

4.2.5.1 Error log no. 1.

Data signal	MFbus signal
MD31	$LOCK_0$
MD30	LOGALL
MD29	BA31
MD28	BA30
MD27	BA29
MD26	BA28
MD25	BA27
MD24	BA26
MD23	BA25
MD22	BA24
MD21	BA23
MD20	BA22
MD19	BA21
MD18	BA20
MD17	BA19
MD16	BA18
MD15	BA17
MD14	BA16
MD13	BA15
MD12	BA14
MD11	BA13
MD10	BA12
MD09	BA11
MD08	BA10
MD07	BA09
MD06	BA08
MD05	BA07
MD04	BA06
MD03	BA05
MD02	BA04
MD01	BA03
MD00	BA02

4.2.5.2 Error log no. 2.

Data signal	MFbus signal
MD31	BBYTE3
MD30	BBYTE2
MD29	BBYTE1
MD28	BBYTE0
MD27	BMORE
MD26	BREAD
MD25	BWRITE
MD24	BWCHK
MD23	BDERR1
MD22	BDERR0
MD21	BERROR
MD20	BFATAL
MD19	BDRYERR
MD18	BDRQERR
MD17	BARYERR
MD16	BCYCLE2
MD15	BCYCLE1
MD14	BCYCLE0
MD13	BSCOD4
MD12	BSCOD3
MD11	BSCOD2
MD10	BSCOD1
MD9	BSCOD0
MD8	BGLOBAL
MD7	BLOCAL
MD6	BMCOD4
MD5	BMCOD3
MD4	BMCOD2
MD3	BMCOD1
MD2	BMCOD0
MD1	BPIRAT
MD0	BREF

4.2.5.3 Error log no. 3.

Data signal	MFbus signal
MD31	Not used
MD30	BSYN6
MD29	BSYN5
MD28	BSYN4
MD27	BSYN3
MD26	BSYN2
MD25	BSYN1
MD24	BSYN0
MD23	
MD22	
MD21	
MD20	
MD19	
MD18	
MD17	
MD16	
MD15	
MD14	
MD13	
MD12	
MD11	
MD10	
MD9	
MD8	
MD7	
MD6	
MD5	
MD4	
MD3	
MD2	
MD1	
MD0	

4.3 The BADAP.

Since James is including two sets of Limit RAMs (one for the internal processor and one for ND100 port), the bits DIB0 and DIB1 in the Badap is used. When the MFcontroller wants to write the Limit Ram local to the ND100 port it must use DIB1 and DIB0.

If the ND100 port is used no other slots can use $MRQ_0 8$.

4.4 Watch-dog time-out function.

An additional function of the Domino watch-dog is inserted on James. Std. Domino watch-dog function is that if a time-out occures, reset from Octobus is enabled. This will also happen in James if the signal

ENWTOC is not set. If ENWTOC is once set a local reset is performed if a time-out occures (its not waiting for Octobus reset). It is not possible to turn of the signal ENWTOC if it set.

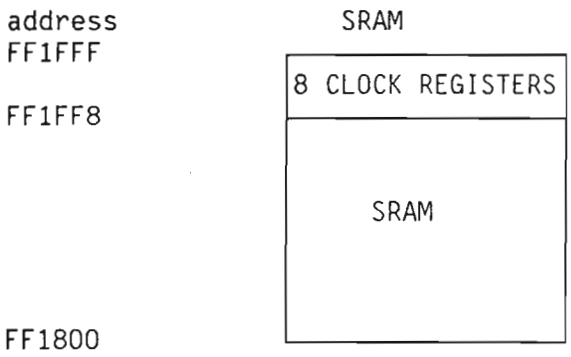
4.5 The second consoll.

The second consoll is handled with the UART2. The terminal signals are RSRXD1 (plug Da11) and RSTXD1 (plug Dc11). The consoll os RS232.

4.6 The SRAM.

The SRAM is 2k x 8byte RAM with a clock and battery back-up.

Eight locations are reserved the clock function. The address and function is given as:



The clock registers with coresponding addresses are:

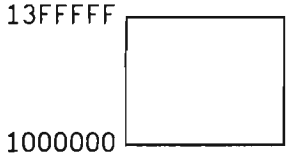
address	clock register	
FF1FFF	year	(00-99)
FF1FFE	month	(01-12)
FF1FFD	date	(01-31)
FF1FFC	day	(01-07)
FF1FFB	hour	(00-23)
FF1FFA	minutes	(00-59)
FF1FF9	seconds	(00-59)
FF1FF8	control	

The format of the different registers are given in "MK48T02 component description".

The lifetime of the battery depends upon the use of the clock. If the clock is diabled when power-down the liftime is estimated to > 30 years. This is independent of the number of power-down and for how long the power-down is. If the clock is enabled during power-down the lifetime is dependent upon the percentage of power-down. If power-down is 100% of the time, the lifetime is 3,6 years.

5. MFbus IO-cycles.

The internal address space on James for I/O cycles is:



~~Egen bootprom~~ Slot no 1 : 1142000H
~~Slot no. 7~~ : 114E000H
5 : 1144000H

MFbus IO-cycles are addressed from the controller as follows:

MCA

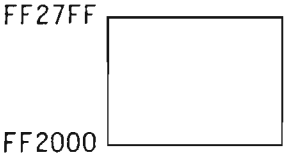
31 25	24	23	22	21 19	18	17 13	12 7	6	5 2	0
0	1	0	0	BCYCLE(2:0)	$BLOCAL_0$	slot no.	mod.typ	0	comm.	

The address bits from 17 to 0 is described in "MULTIPORT MEMORY 5 DESCRIPTION".

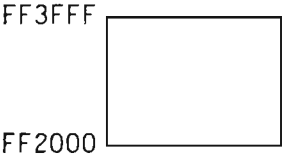
BCYCLE : 1 bit på byte no. 5 + 2 bit på nästa
BLOCAL : nästnäst bitar på no 5
Slot no : 3 bitar på no 4 + 2 på no 5
mod.typ : 4 bitar på no 2 + hela 3 + första på 4

6. The EEPROM in the backwiring.

The EEPROM is in James local address space:



The EEPROM is 2k byte. There is also a possibility to make it greater, 8k byte. The address space is then:



A write to certain locations in the EEPROM must be protected one way or the other. To ensure that two write pulses have 10ms time difference, the interrupts from counter TB on the MFP is used (see " MFP description" below).

7. Interrupt description.

Several interrupts to the MFP (MC68901) is a part of the Domino Device. The interrupts on James are:

GPIO0 : Not used.
GPIO1 : LOAD signal from the ND100 bus.
GPIO2 : EEINT. A write to the local EEPROM is finnished (std.Domino)
GPIO3 : $DMATRAP_0$. Trap when device running DMA.
GPIO4 : MCL from the ND100 bus.
GPIO5 : $INTL_0$. Interrupt from the MFbus error logs.

GPIO6 : $UARTINT_0$. From the second UART.
GPIO7 : $POERR_0$. An error from the BADAP, when ND port is accessing the MFbus has occured.

The interrupts connected direct to the processor is:

LEVEL 2 : Interrupt from the MFP.
LEVEL 3 : TCO. James timer interrupt.
LEVEL 4 : Ethernet interrupt.
LEVEL 5 : $OCINT_0$ (see std. Domino description).
LEVEL 6 : $IREDY_0$ (see std. Domino description).
LEVEL 7 : $INT7_0$ (see std. Domino description).

8. MFP description.

The MFP must take care of the GPIO interrupt signals listed above. The timer A and D is std. Domino. Timer B, C is spesific for James.

8.1 Timer B.

It is used for giving time refference to the loadmeter and handle the time between several write pulses to the EEPROM in the backwiring. The way it should opperate is to give interrupts with a certain frequency. The processes to handle the loadmeter and write's to the EEPROM must count the number of interrupts and decide what to do and when to do it.

8.2 Timer C.

This timer is used to give interrupts on Level 3 to the processor.

9. MFP description.

The MFP must handle the GPIO interrupts given above. Two of the timers on the MFP, TA and TD is std. Domino. The two other, TB and TC is spesific to James.

9.1 Timer TB.

The timer TB must be programmed to give interrupts at a given frequency. It is used for giving time reference for the loadmeter and write pulses for the EEPROM in the backwiring. The processes for the

two tasks must take care of the counting of number of interrupts, what to do and when to do it.

9.2 Timer TC.

This timer gives interrupts on Level 3 on the processor. It's use is generating scheduler interrupts to processors.

10. ND100 port.

The NDport function is nearly the same as on the DBC controller. It consists of three parts:

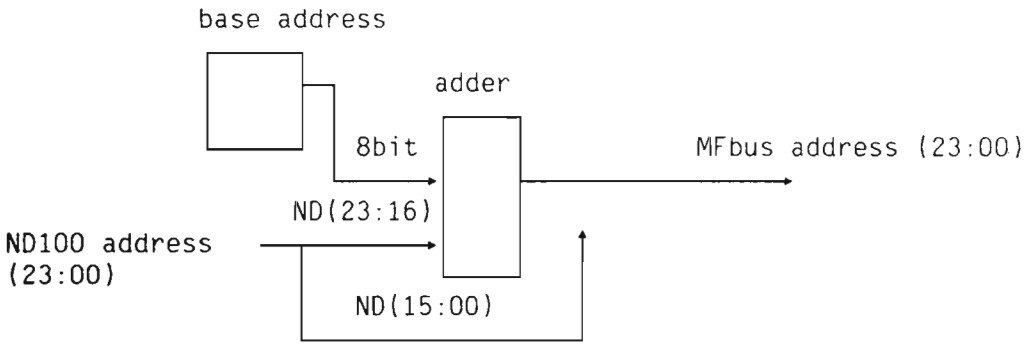
- ND100 MFbus interface.
- ND100 Octobus.
- ND100 termination.

The ND100 port may not be used and therefor not mounted.
The parts are discussed below.

10.1 ND100 MFbus interface.

This is an interface when ND100 is running memory cycles. To decide if ND100 is accessing the MFbus, the address is checked in a Limit RAM. The Limit RAM is set up by the MFbus controller (as the Limit Ram in std. Domino). If the ND100 address is OK the cycle accesses the MFbus. Since the ND100 data width is 23bits wide, the MFbus accesses is always 16bit.

The physical address on MFbus is the ND100 address with an offset:



The ND100 address ND(23:16) is added with a base. This base is set up by the local processor.

The least significant address on the ND00 address is deciding if the MFbus data word is the lower or the upper.

10.2 ND100 port Octobus.

The Octobus is read or written by ND100 IOXE-cycles. There are two reasons for the ND100 CPU to access the Ocotbus on James:

- Ordinary Octobus operation. The device number is selected by a thumbwheel:
  Ordinary IOXE address from ND100: 1004x0 (x is the selected device number.)

- Read a bootstrap from the Octobus. The address is:
  IOXE address if bootstrap : 000400

10.3 ND100 bus termination.

The ND100 bus signals are terminated with 220/330 Ohm.

11. Ethernet.

The Ethernet is the same as Ethernet 3. The only difference is that Ethernet interrupt is on level 4 on the Domino processor.

11.1 Ethernet interface address decoding.

LANCE (7990)	Data (Read and write)	(16bit port)	FF0000 - FF001F
LANCE	Address	(16bit port)	FF0020 - FF003F
Write LANCE address register		(16bit port)	FF0040
Read Ethernet Status Register		(16bit port)	FF0042
Transceiver power	(write)	(16bit port)	FF0046

12. Plug description.

12.1 Plug A.

SIGNALS ON A-CONNECTOR								
PIN. NO.		SIGNAL	PIN. NO.		SIGNAL	PIN.NO.		SIGNAL
Aa	1	GND	Ab	1	GND	Ac	1	GND
Aa	2	5VSTBY	Ab	2	5VSTBY	Ac	2	5VSTBY
Aa	3	$BARQ_0$	Ab	3	$BARY_0$	Ac	3	$BREF_0$
Aa	4	$BTOTRES_0$	Ab	4	$BPFAIL_0$	Ac	4	$BNAVAL_0$
Aa	5	$BDRQ_0$	Ab	5	$BDRY_0$	Ac	5	$BBUSY_0$
Aa	6	$BLOCK_0$	Ab	6	$BEEP_0$	Ac	6	$BPIRAT_0$
Aa	7	$BNINC_0$	Ab	7	$BMORE_0$	Ac	7	$BEOSTR_0$
Aa	8	GND	Ab	8	GND	Ac	8	GND
Aa	9	$BBYTE_0 0$	Ab	9	$BBYTE_0 1$	Ac	9	$BBYTE_0 2$
Aa	10	$BBYTE_0 3$	Ab	10	$BREAD_0$	Ac	10	$BWRITE_0$
Aa	11	$BCYCLE_0 0$	Ab	11	$BCYCLE_0 1$	Ac	11	$BCYCLE_0 2$
Aa	12	$BDRQERR_0$	Ab	12	$BDRYERR_0$	Ac	12	$BARYERR_0$
Aa	13	$BLOCAL_0$	Ab	13	$BGLOBAL_0$	Ac	13	$BREW_0$
Aa	14	$BMCOD_0 0$	Ab	14	$BMCOD_0 1$	Ac	14	$BMCOD_0 2$
Aa	15	$BMCOD_0 3$	Ab	15	$BMCOD_0 4$	Ac	15	$BSCOD_0 0$
Aa	16	$BSCOD_0 1$	Ab	16	$BSCOD_0 2$	Ac	16	$BSCOD_0 3$
Aa	17	$BSCOD_0 4$	Ab	17	$BSLOT_0 0$	Ac	17	$BSLOT_0 1$
Aa	18	$BSLOT_0 2$	Ab	18	$BSLOT_0 3$	Ac	18	$BSLOT_0 4$
Aa	19	GND	Ab	19	GND	Ac	19	GND
Aa	20	BPA_0	Ab	20	$BA_0 00$	Ac	20	$BA_0 01$
Aa	21	$BA_0 02$	Ab	21	$BA_0 03$	Ac	21	$BA_0 04$
Aa	22	$BA_0 05$	Ab	22	$BA_0 06$	Ac	22	$BA_0 07$
Aa	23	$BA_0 08$	Ab	23	$BA_0 09$	Ac	23	$BA_0 10$
Aa	24	$BA_0 11$	Ab	24	$BA_0 12$	Ac	24	$BA_0 13$
Aa	25	$BA_0 14$	Ab	25	$BA_0 15$	Ac	25	$BA_0 16$
Aa	26	$BA_0 17$	Ab	26	$BA_0 18$	Ac	26	$BA_0 19$
Aa	27	$BA_0 20$	Ab	27	$BA_0 21$	Ac	27	$BA_0 22$
Aa	28	$BA_0 23$	Ab	28	$BA_0 24$	Ac	28	$BA_0 25$
Aa	29	$BA_0 26$	Ab	29	$BA_0 27$	Ac	29	$BA_0 28$
Aa	30	$BA_0 29$	Ab	30	$BA_0 30$	Ac	30	$BA_0 31$
Aa	31	VCC	Ab	31	VCC	Ac	31	VCC
Aa	32	GND	Ab	32	GND	Ac	32	GND

12.2 Plug B.

SIGNALS ON B-CONNECTOR								
PIN. NO.		SIGNAL	PIN. NO.		SIGNAL	PIN.NO.		SIGNAL
Ba	1	(+12V) **	Bb	1	GND	Bc	1	(+12V)**
Ba	2	(+12V) **	Bb	2	GND	Bc	2	
Ba	3		Bb	3	VCC	Bc	3	
Ba	4		Bb	4	VCC	Bc	4	
Ba	5		Bb	5	$BD_0$00	Bc	5	
Ba	6		Bb	6	$BD_0$01	Bc	6	
Ba	7		Bb	7	$BD_0$02	Bc	7	
Ba	8		Bb	8	$BD_0$03	Bc	8	
Ba	9		Bb	9	$BD_0$04	Bc	9	
Ba	10		Bb	10	$BD_0$05	Bc	10	
Ba	11		Bb	11	$BD_0$06	Bc	11	
Ba	12	CD	Bb	12	$BD_0$07	Bc	12	CD_0
Ba	13	TD	Bb	13	$BD_0$08	Bc	13	TD_0
Ba	14		Bb	14	$BD_0$09	Bc	14	
Ba	15	RD	Bb	15	$BD_0$10	Bc	15	RD_0
Ba	16		Bb	16	$BD_0$11	Bc	16	EXTPOWER
Ba	17		Bb	17	$BD_0$12	Bc	17	
Ba	18		Bb	18	$BD_0$13	Bc	18	
Ba	19		Bb	19	$BD_0$14	Bc	19	
Ba	20		Bb	20	$BD_0$15	Bc	20	
Ba	21		Bb	21	$BD_0$16	Bc	21	
Ba	22	$MGR_0$15	Bb	22	$BD_0$17	Bc	22	$MGR_0$14
Ba	23	$MGR_0$13	Bb	23	$BD_0$18	Bc	23	$MGR_0$12
Ba	24	$MGR_0$11	Bb	24	$BD_0$19	Bc	24	$MGR_0$10
Ba	25	$MGR_0$09	Bb	25	$BD_0$20	Bc	25	$MGR_0$08
Ba	26	$MGR_0$07	Bb	26	$BD_0$21	Bc	26	$MGR_0$06
Ba	27	$MGR_0$05	Bb	27	$BD_0$22	Bc	27	$MGR_0$04
Ba	28	$MGR_0$03	Bb	28	$BD_0$23	Bc	28	$MGR_0$02
Ba	29	$MGR_0$01	Bb	29	MGR_0	Bc	29	
Ba	30		Bb	30	5VSTBY	Bc	30	
Ba	31	GND *	Bb	31	GND	Bc	31	GND *
Ba	32	+12V *	Bb	32	GND	Bc	32	+12V *

* NOT USED ON THE PROTOTYPE PRINT.
** ON THE B-VERSION THESE SHOULD NOT BE USED (USE INSTEAD Ba32 AND Bc32).

12.3 Plug C.

SIGNALS ON C-CONNECTOR								
PIN. NO.		SIGNAL	PIN. NO.		SIGNAL	PIN.NO.		SIGNAL
Ca	1		Cb	1	GND	Cc	1	
Ca	2		Cb	2	GND	Cc	2	
Ca	3		Cb	3	VCC	Cc	3	
Ca	4		Cb	4	VCC	Cc	4	
Ca	5	MDO3	Cb	5	$BD_0$24	Cc	5	GND
Ca	6	MDO4	Cb	6	$BD_0$25	Cc	6	MDO2
Ca	7	MDO5	Cb	7	$BD_0$26	Cc	7	MDO1
Ca	8	MDO6	Cb	8	$BD_0$27	Cc	8	MDO0
Ca	9	MDO7	Cb	9	$BD_0$28	Cc	9	MCA00
Ca	10	$8255CE_0$	Cb	10	$BD_0$29	Cc	10	MCA01
Ca	11	MCA10	Cb	11	$BD_0$30	Cc	11	MCA02
Ca	12	$RDEE_0$	Cb	12	$BD_0$31	Cc	12	MCA03
Ca	13	$WREE_0$	Cb	13	$BP_0$0	Cc	13	MCA04
Ca	14	MCA09	Cb	14	$BP_0$1	Cc	14	MCA05
Ca	15	MCA08	Cb	15	$BP_0$2	Cc	15	MCA06
Ca	16	VCC	Cb	16	$BP_0$3	Cc	16	MCA07
Ca	17	MCA11*	Cb	17	$BSYN_0$0	Cc	17	MCA12*
Ca	18		Cb	18	$BSYN_0$1	Cc	18	$EEBSY_0$*
Ca	19		Cb	19	$BSYN_0$2	Cc	19	
Ca	20		Cb	20	$BSYN_0$3	Cc	20	
Ca	21		Cb	21	$BSYN_0$4	Cc	21	
Ca	22	$MRQ_0$15	Cb	22	$BSYN_0$5	Cc	22	$MRQ_0$14
Ca	23	$MRQ_0$13	Cb	23	$BSYN_0$6	Cc	23	$MRQ_0$12
Ca	24	$MRQ_0$11	Cb	24	$BFATAL_0$	Cc	24	$MRQ_0$10
Ca	25	$MRQ_0$09	Cb	25	$BERROR_0$	Cc	25	$MRQ_0$08
Ca	26	$MRQ_0$07	Cb	26	$BDERR_0$0	Cc	26	$MRQ_0$06
Ca	27	$MRQ_0$05	Cb	27	$BDERR_0$1	Cc	27	$MRQ_0$04
Ca	28	$MRQ_0$03	Cb	28	$BWCHK_0$	Cc	28	$MRQ_0$02
Ca	29	$MRQ_0$01	Cb	29	MRQ_0	Cc	29	
Ca	30		Cb	30	5VSTBY	Cc	30	
Ca	31	GND **	Cb	31	GND	Cc	31	GND **
Ca	32	+12V **	Cb	32	GND	Cc	32	+12V **

* For future use with 8k byte EEPROM.
** NOT USED ON THE PROTOTYPE PRINT.

12.4 Plug D.

SIGNALS ON D-CONNECTOR								
PIN.	NO.	SIGNAL	PIN.	NO.	SIGNAL	PIN.	NO.	SIGNAL
Da	1	$XCLK_0$	Db	1	GND	Dc	1	XCLK
Da	2	$XDAT_0$	Db	2	GND	Dc	2	XDAT
Da	3	$XREQ_0$	Db	3	VCC	Dc	3	XREQ
Da	4	$XRFO_0$	Db	4	VCC	Dc	4	XRFO
Da	5	GND	Db	5	$NBREF_0$	Dc	5	$XFAIL_0$
Da	6	PUP0	Db	6	$BAPR_0$	Dc	6	$PDWN_0 0$
Da	7	PUP1	Db	7	$BINOXE_0$	Dc	7	$PDWN_0 1$
Da	8	PUP2	Db	8	$INIDENT_0$	Dc	8	$PDWN_0 2$
Da	9	PUP3	Db	9	$BINT_0 13$	Dc	9	$PDWN_0 3$
Da	10	GND	Db	10	$BDAP_0$	Dc	10	$LOAD_0$
Da	11	RSRXD1	Db	11		Dc	11	RSTXD1
Da	12	RES	Db	12	$TXREQ_0$	Dc	12	RSTXD
Da	13	RES	Db	13	$TXDAT_0$	Dc	13	RSRXD
Da	14	RES	Db	14	RREQ	Dc	14	RES
Da	15	RES	Db	15	RCLK	Dc	15	
Da	16		Db	16	RDAT	Dc	16	
Da	17	RES	Db	17	ROSC	Dc	17	GND
Da	18	$NBDRY_0$	Db	18	$NBERROR_0$	Dc	18	$BMEM_0$
Da	19	$NBD_0 01$	Db	19	$NBD_0 16$	Dc	19	$NBD_0 00$
Da	20	$NBD_0 03$	Db	20	$NBD_0 17$	Dc	20	$NBD_0 02$
Da	21	$NBD_0 05$	Db	21	$NBD_0 18$	Dc	21	$NBD_0 04$
Da	22	$NBD_0 07$	Db	22	$NBD_0 19$	Dc	22	$NBD_0 06$
Da	23	$NBD_0 09$	Db	23	BVPP	Dc	23	$NBD_0 08$
Da	24	$NBD_0 11$	Db	24		Dc	24	$NBD_0 10$
Da	25	$NBD_0 13$	Db	25	RCLK16	Dc	25	$NBD_0 12$
Da	26	$NBD_0 15$	Db	26		Dc	26	$NBD_0 14$
Da	27	$BPARERR_0$	Db	27	$NBD_0 20$	Dc	27	$NBD_0 22$
Da	28	$BSMRQ_0$	Db	28	$NBD_0 21$	Dc	28	$NBD_0 23$
Da	29	$BINPUT_0$	Db	29	5VSTBY	Dc	29	$BMCL_0$
Da	30		Db	30	5VSTBY	Dc	30	
Da	31	SCLK	Db	31	GND	Dc	31	
Da	32	$XFAIL_0$	Db	32	GND	Dc	32	

NOTE : RES is reserved pins.