

Integrated Device Technology, Inc.

CMOS STATIC RAMs 64K (16K x 4-BIT) Separate Data Inputs and Outputs

IDT71981S/L
IDT71982S/L

FEATURES:

- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
 - Military: 20/25/35/45/55/70/85ns (max.)
 - Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin hermetic and plastic DIP, 28-pin leadless chip carrier, and 28-pin SOJ
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CMOS.

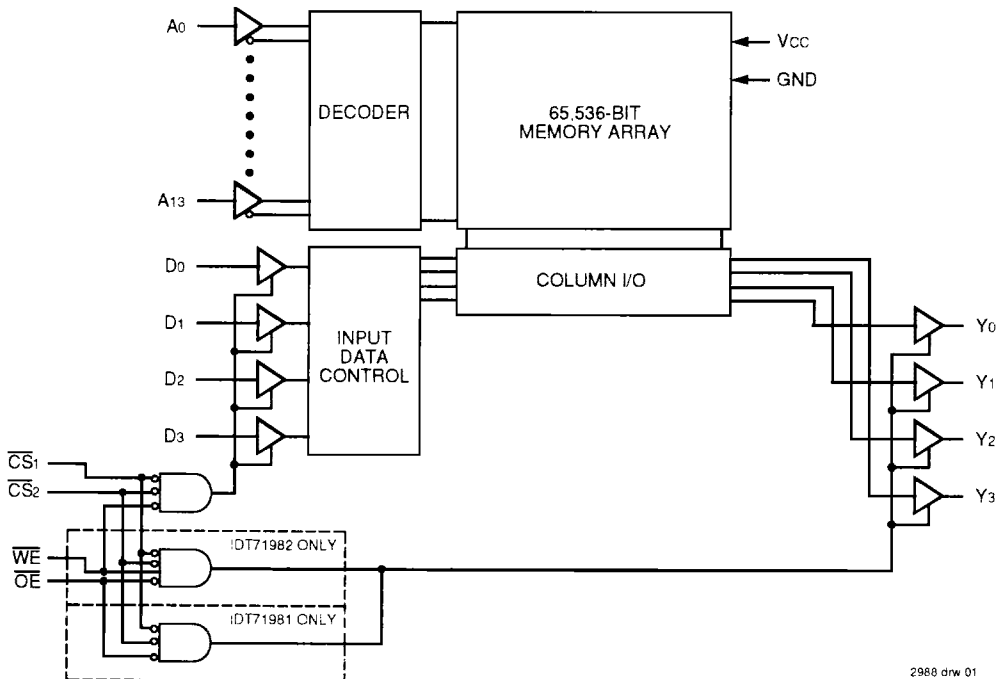
Access times as fast as 15ns are available. These circuits also offer a reduced power standby mode (ISB). When \overline{CS}_1 or \overline{CS}_2 goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra-low-power standby mode (ISB1), the devices consume less than 2.5mW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 30 μ W operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply.

The IDT71981/IDT71982 are packaged in either a 28-pin, 300 mil hermetic DIP, 28-pin 300 mil plastic DIP, 28-pin SOJ, or 28-pin leadless chip carrier.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



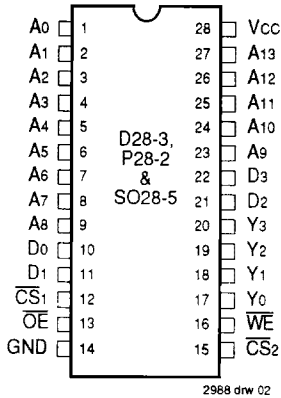
2988 drw 01

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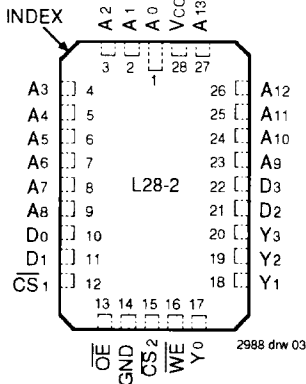
MILITARY AND COMMERCIAL TEMPERATURE RANGES

SEPTEMBER 1992

PIN CONFIGURATIONS



**DIP/SOJ
 TOP VIEW**



**LCC
 TOP VIEW**

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
COU	Output Capacitance	VOUT = 0V	7	pF

NOTE:
 1. This parameter is determined by device characterization, but is not production tested.

PIN DESCRIPTIONS

Name	Description
A0-A13	Address Inputs
CS1, CS2	Chip Selects
WE	Write Enable
OE	Output Enable
D0-D3	DATAIN
Y0-Y3	DATAOUT
VCC	Power
GND	Ground

2988 tbi 01

TRUTH TABLE⁽³⁾

Mode	CS1	CS2	WE	OE	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	DOUT	Active
Write ⁽¹⁾	L	L	L	L	DIN	Active
Write ⁽¹⁾	L	L	L	H	High Z	Active
Write ⁽²⁾	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

NOTES:

- For IDT71981 only.
- For IDT71982 only.
- H = VIH, L = VIL, X = don't care.

2988 tbi 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2988 tbi 03



RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE: 2988 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2988 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71981/2S		IDT71981/2L		Unit	
			Min.	Max.	Min.	Max.		
I _{IU}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	MIL. COM'L.	— 10 5	— —	5 2	μA	
I _{LO}	Output Leakage Current	V _{CC} = Max., $\overline{CS}_{1,2} = V_{IH}$, V _{OUT} = GND to V _{CC}	MIL. COM'L.	— 10 5	— —	5 2	μA	
V _{OL}	Output Low Voltage	I _{OL} = 10mA, V _{CC} = Min.		—	0.5	—	0.5	V
		I _{OL} = 8mA, V _{CC} = Min.		—	0.4	—	0.4	
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min.		2.4	—	2.4	—	V

2988 tbl 07

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71981/2S15		71981/2S20		71981/2S25		71981/2S35		71981/2S45		71981/2S55/70		71981/2S85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC1}	Operating Power Supply Current $\overline{CS}_{1,2} = V_{IL}$, Outputs Open V _{CC} = Max., f = 0 ⁽²⁾	S	100	—	100	105	100	105	100	105	—	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	—	80	
I _{CC2}	Dynamic Operating Current $\overline{CS}_{1,2} = V_{IL}$, Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾	S	135	—	130	160	125	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	125	105	115	—	110	—	110	—	105	
I _{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_{1,2} \geq V_{IH}$, V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽²⁾	S	60	—	55	70	50	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	50	30	40	—	35	—	35	—	35	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}_{1,2} \geq V_{HC}$, V _{CC} = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 ⁽²⁾	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

- All values are maximum guaranteed values.
- At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

2988 tbl 08

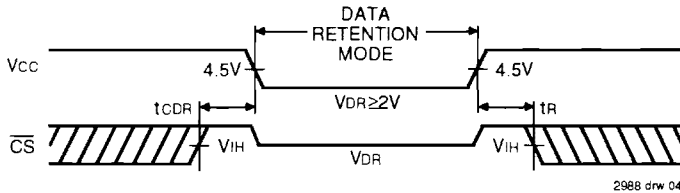
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0v	3.0V	2.0V	3.0V	
VDR	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
ICCDR	Data Retention Current	MIL. COM.L.	—	10	15	600	900	μA
			—	10	15	150	225	
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time	$\overline{CS}1$ or $\overline{CS}2 \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	0	—	—	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	—	—	ns
I _{LI} ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

- NOTES:**
- TA = +25°C.
 - t_{RC} = Read Cycle Time.
 - This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2988 tbl 10

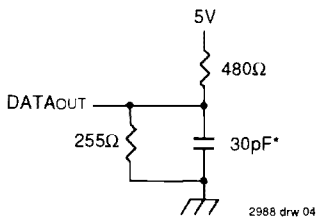


Figure 1. AC Test Load

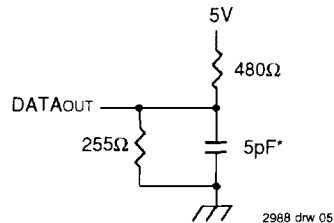


Figure 2. AC Test Load
 (for t_{CLZ1, 2}, t_{OLZ}, t_{CHZ1, 2}, t_{OHZ}, t_{ow} and t_{whz})

*Includes scope and jig capacitances

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

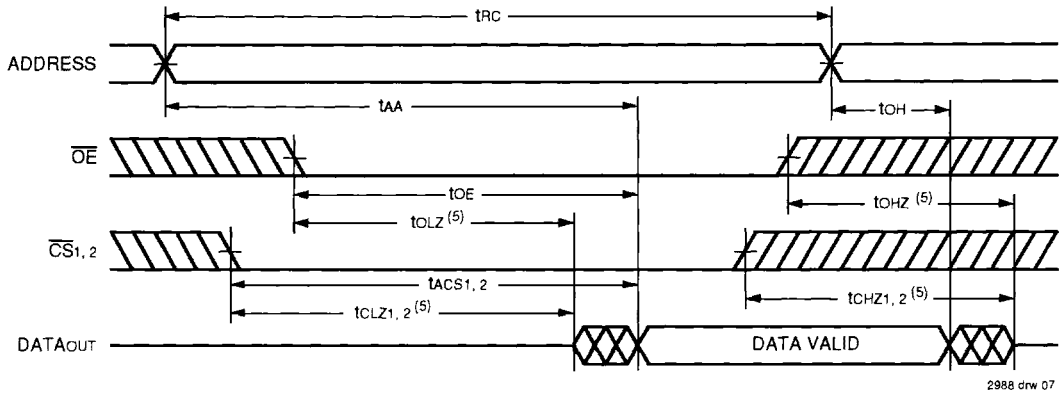
Symbol	Parameter	71981/2S15 ⁽¹⁾ /20		71981/2S25		71981/2S35/45 ⁽²⁾		71981/2S55 ⁽²⁾		71981/2S70 ⁽²⁾		71981/2S85 ⁽²⁾		Unit
		71981/2L15 ⁽¹⁾ /20		71981/2L25		71981/2L35/45 ⁽²⁾		71981/2L55 ⁽²⁾		71981/2L70 ⁽²⁾		71981/2L85 ⁽²⁾		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t _{RC}	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
t _{AA}	Address Access Time	—	15/19	—	25	—	35/45	—	55	—	70	—	85	ns
t _{ACS1,2}	Chip Select-1,2 Access Time ⁽³⁾	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
t _{CLZ1,2}	Chip Select-1,2 to Output in Low-Z ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{OE}	Output Enable to Output Valid	—	8/9	—	11	—	20/25	—	35	—	45	—	55	ns
t _{OLZ}	Output Enable to Output in Low-Z ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{CHZ1,2}	Chip Select1,2 to Output in High-Z ⁽⁴⁾	—	7/8	—	10	—	4	—	20	—	25	—	30	ns
t _{OHZ}	Output Disable to Output in High-Z ⁽⁴⁾	—	7/8	—	9	—	15	—	20	—	25	—	30	ns
t _{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{PU}	Chip Select to Power-Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Deselect to Power-Down Time ⁽⁴⁾	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns

NOTES:

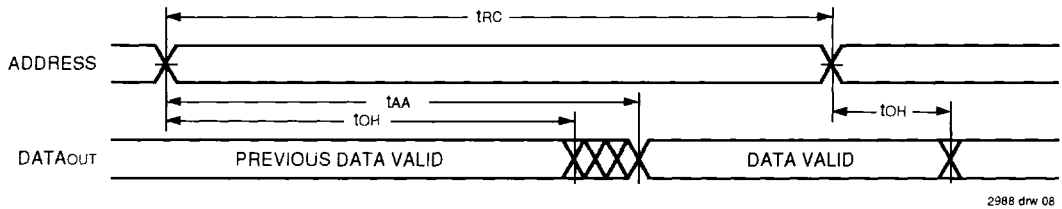
- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- Both chip selects must be active low for the device to be selected.
- This parameter is guaranteed by device characterization, but is not production tested.

2988 tbl 11

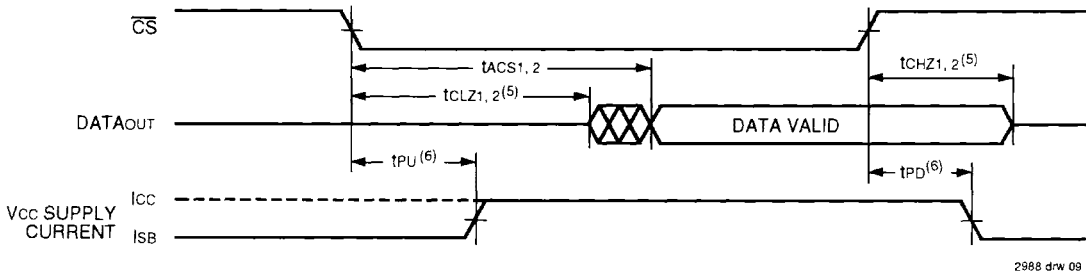
TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)



NOTES:

1. \overline{WE} is HIGH for READ cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with \overline{CS}_1 and or \overline{CS}_2 transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200mV$ from steady state voltage.
6. This parameter is guaranteed by device characterization but is not production tested.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

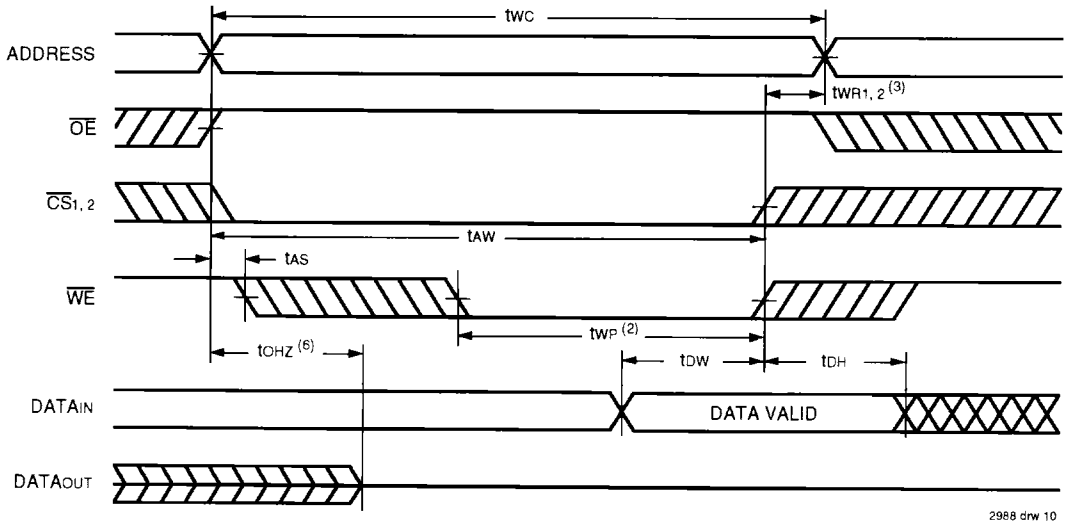
Symbol	Parameter	71981/2S15 ⁽¹⁾ /20 71981/2L15 ⁽¹⁾ /20		71981/2S25 71981/2L25		71981/2S35/45 ⁽²⁾ 71981/2L35/45 ⁽²⁾		71981/2S55 ⁽²⁾ 71981/2L55 ⁽²⁾		71981/2S70 ⁽²⁾ 71981/2L70 ⁽²⁾		71981/2S85 ⁽²⁾ 71981/2L85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	14/17	—	20	—	30/40	—	50	—	60	—	75	—	ns
tCW1,2	Chip Select to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAW	Address Valid to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tWR1,2	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z ^(3,5)	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
tDW	Data Valid to End of Write	10/10	—	13	—	15/20	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write ^(3,5)	5	—	5	—	5	—	5	—	5	—	5	—	ns
tVY	Data Valid to Output Valid ^(3,4)	—	12/15	—	20	—	30/35	—	40	—	45	—	50	ns
tWY	Write Enable to Output Valid ^(3,4)	—	12/15	—	20	—	30/35	—	40	—	45	—	50	ns

NOTES:

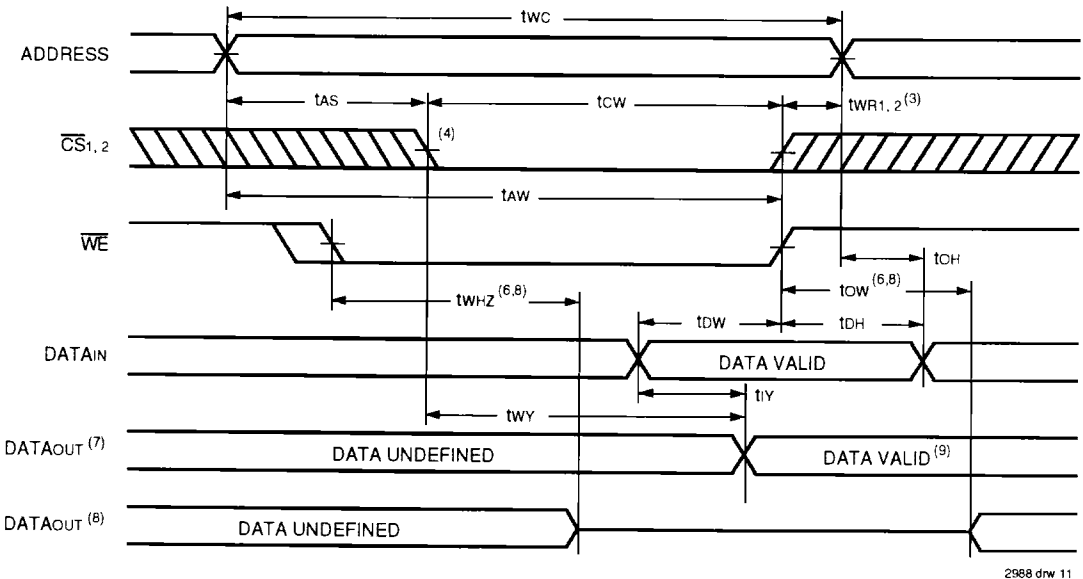
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.

2988 tbl 12

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)⁽¹⁾



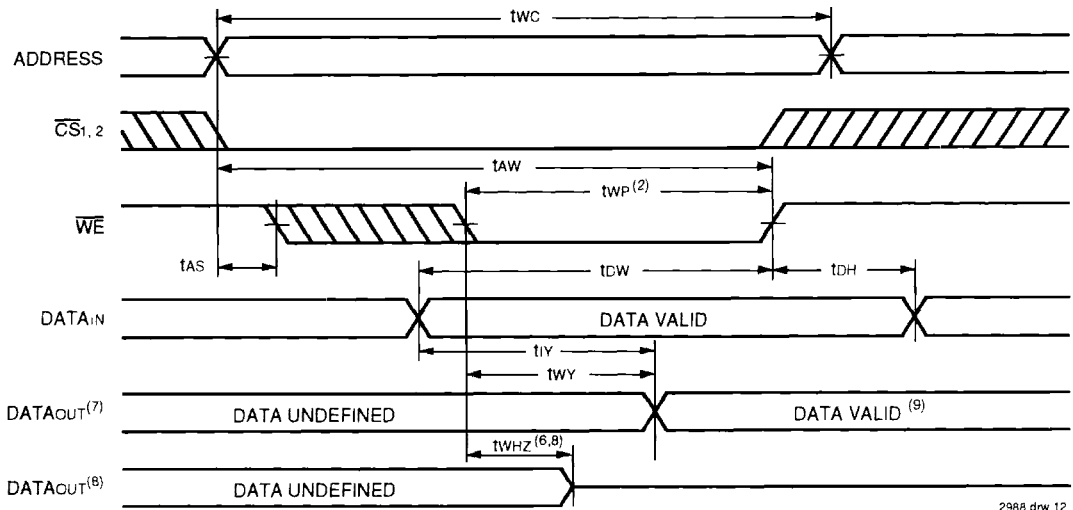
TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1, 5)



NOTES:

1. \overline{WE} or \overline{CS}_1 or \overline{CS}_2 must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW \overline{WE} , a LOW \overline{CS}_1 and a low \overline{CS}_2 .
3. t_{WR} is measured from the earlier of \overline{CS}_1 , \overline{CS}_2 or \overline{WE} going HIGH to the end of the write cycle.
4. If the \overline{CS}_1 and/or \overline{CS}_2 low transition occurs simultaneously with or after the \overline{WE} low transition, outputs remain in a high-impedance state.
5. \overline{OE} is continuously LOW ($\overline{OE} = V_{IL}$).
6. Transition is measured $\pm 200mV$ from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. $DATA_{OUT} = DATA_{IN}$.

TIMING WAVEFORM OF WRITE CYCLE NO. 3 (\overline{WE} CONTROLLED, \overline{OE} LOW)^(1, 5)



2988 drw 12

NOTES:

1. \overline{WE} or \overline{CS}_1 or \overline{CS}_2 must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW \overline{WE} , a low \overline{CS}_1 and a LOW \overline{CS}_2 .
3. t_{WR} is measured from the earlier of \overline{CS}_1 , \overline{CS}_2 or \overline{WE} going HIGH to the end of the write cycle.
4. If the \overline{CS}_1 and or \overline{CS}_2 low transition occurs simultaneously with or after the \overline{WE} low transition, outputs remain in a high-impedance state.
5. \overline{OE} is continuously LOW ($\overline{OE} = V_L$).
6. Transition is measured $\pm 200mV$ from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. $DATA_{OUT} = DATA_{IN}$.

ORDERING INFORMATION

IDT	XXXX	X	XX	XX	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C)
					B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
					D	300 mil CERDIP (D28-3)
					P	300 mil Plastic DIP (P28-2)
					L	Leadless Chip Carrier (L28-2)
					Y	300 mil Small Outline IC, J-Bend (SO28-5)
					15	Commercial Only
					20	
					25	
					35	
					45	
					55	Military Only
					70	
					85	
					85	
					S	Standard Power
					L	Low Power
					71981	64K (16K x 4-Bit)
					71982	64K (16K x 4-Bit) High Impedance Outputs

2988 drw 13