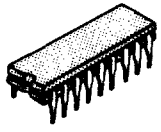
HM511001 Series

1048576-word x 1-bit CMOS Dynamic Random Access Memory

The Hitachi HM511001 Series is a CMOS dynamic RAM organized 1,048,576-word x 1-bit. HM511001 has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM511001, offers Nibble Mode as a high speed access mode.

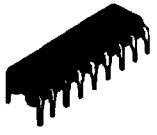
Multiplexed address input permits the HM511001 to be packaged in standard 18-pin plastic DIP, CERDIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM511001 Series



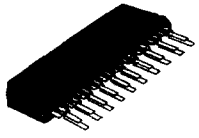
(DG-18A)

HM511001P Series



(DP-18C)

HM511001ZP Series



(ZP-20)

HM511001JP Series

(CP-20D)

■ FEATURES

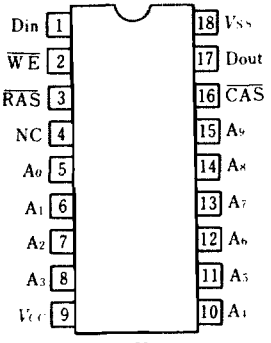
- High Speed: Access Time 100/120ns (max.)
- Low Power: 300mW (active), 10mW (standby)
- Nibble mode capability
- 512 refresh cycles . . . (8ms)
- 3 variations of refresh: $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM511001-10 HM511001-12	100ns 120ns	300 mil 18 pin CERDIP
HM511001P-10 HM511001P-12	100ns 120ns	300 mil 18 pin Plastic DIP
HM511001ZP-10 HM511001ZP-12	100ns 120ns	20 pin plastic ZIP
HM511001JP-10 HM511001JP-12	100ns 120ns	20 pin Plastic SOJ

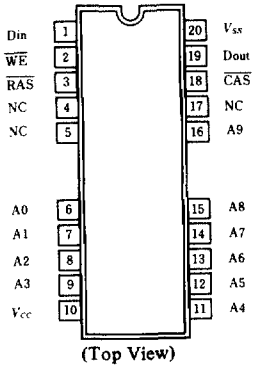
■ PIN ARRANGEMENT

- HM511001 Series,
  HM511001P Series



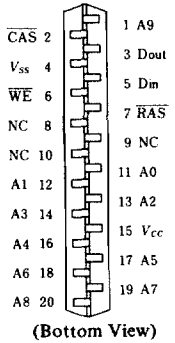
(Top View)

- HM511001JP Series



(Top View)

- HM511001ZP Series



(Bottom View)

HITACHI

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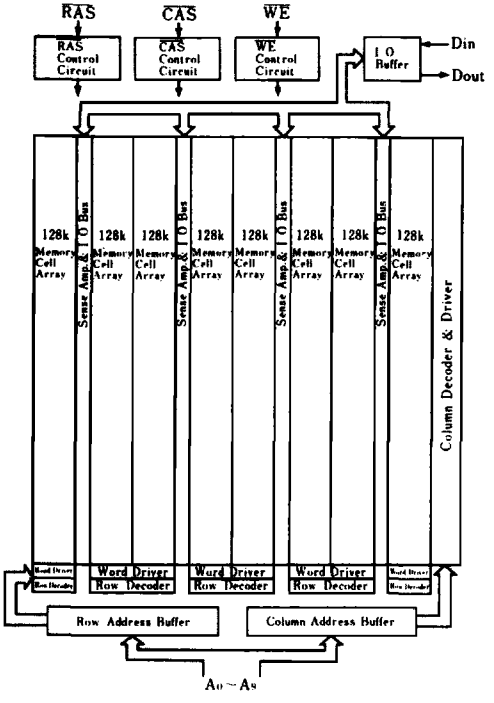
■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, T_a (Ambient) . . . . . 0 to +70°C
Storage Temperature (Plastic) . . . . . −55 to +125°C
Storage Temperature (Cerdip) . . . . . −65 to +150°C
Power dissipation 1W
Short circuit output current 50mA

$A_0 - A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_8$	Refresh Address Inputs

■ BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	–	6.5	V	1
Input Low voltage	V_{IL}	−2.0	–	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	Test Condition		HM511001-10 min.	HM511001-10 max.	HM511001-12 min.	HM511001-12 max.	Unit	Note
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = min.		–	60	–	50	mA	1
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	TTL interface	–	2	–	2	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC}-0.2V, Dout = High-Z	CMOS interface	–	1	–	1		
Refresh Current	I_{CC3}	$\overline{RAS}$ only Refresh, t_{RC} = min.		–	50	–	40	mA	
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout Enable		–	5	–	5	mA	1
Refresh Current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC} = min.		–	50	–	40	mA	
Nibble Mode Supply Current	I_{CC8}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{NC} = min.		–	50	–	45	mA	
Input Leakage	I_{LI}	V_{in} = 0 to +7V		-10	10	-10	10	μA	
Output Leakage	I_{LO}	V_{out} = 0 to +7V, Dout is disabled		-10	10	-10	10	μA	
Output Levels	V_{OH}	I_{out} = -5 mA		2.4	V_{CC}	2.4	V_{CC}	V	
	V_{OL}	I_{out} = 4.2 mA		0	0.4	0	0.4	V	

Note) *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (V_{CC} = 5V ±10%, T_a = 25°C)

Parameter		Symbol	typ.	max.	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1, 2
Output Capacitance	Data-out	C_o	–	7		

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (V_{CC}=5V ±10%, V_{SS} = 0V, T_a = 0 to +70°C)[1),10)]

Parameter	Symbol	HM511001-10 min.	HM511001-10 max.	HM511001-12 min.	HM511001-12 max.	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	2, 3
Output Buffer Turn-off Delay	t_{OFF}	–	25	–	30	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	ns	7
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	ns	

(to be continued)

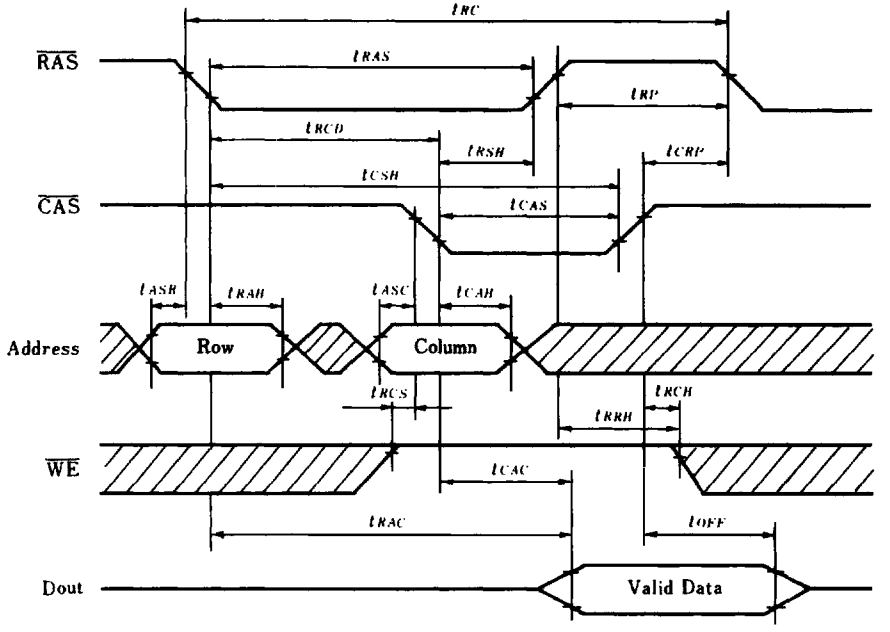
Parameter	Symbol	HM511001-10		HM511001-12		Unit	Note
		min.	max.	min.	max.		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	ns	
Data-in-Setup Time	t_{DS}	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	ns	9
Read Command Setup Time	t_{RCS}	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	
Refresh Period	t_{REF}	–	8	–	8	ms	
Read-Write Cycle Time	t_{RWC}	220	–	255	–	ns	
Read Modify Write Cycle Time	t_{RWS}	140	–	165	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	90	–	110	–	ns	8
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	–	50	–	ns	8
$\overline{CAS}$ Setup Time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	–	25	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	ns	
Nibble Mode Access Time	t_{NAC}	–	30	–	35	ns	
Nibble Mode Cycle Time	t_{NC}	50	–	55	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	–	10	–	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	30	–	35	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	40	–	50	–	ns	
Nibble Mode Read Modify Write Cycle Time	$tNRWC$	65	–	75	–	ns	
Nibble Mode Write Command $\overline{CAS}$ Read Time	$tWCWL$	20	–	25	–	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay Time	$tNCWD$	20	–	25	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
5. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.

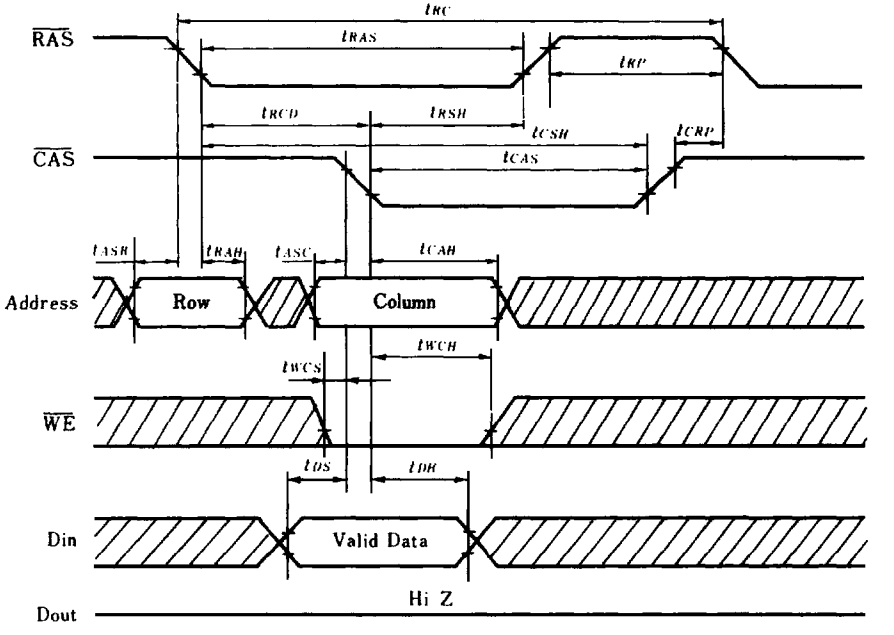
■ TIMING WAVEFORMS

• Read Cycle



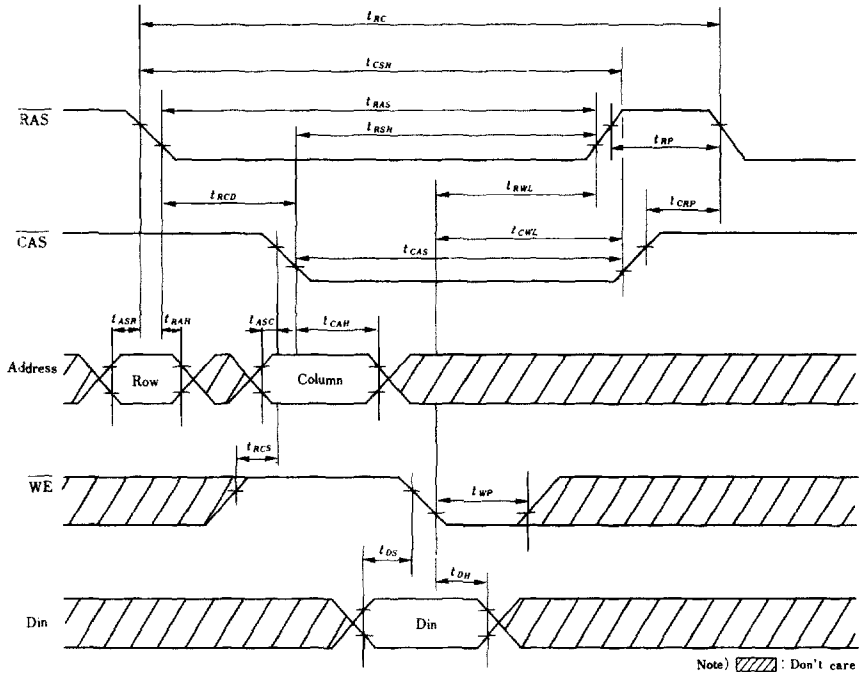
Note) ▨: Don't care

• Early Write Cycle

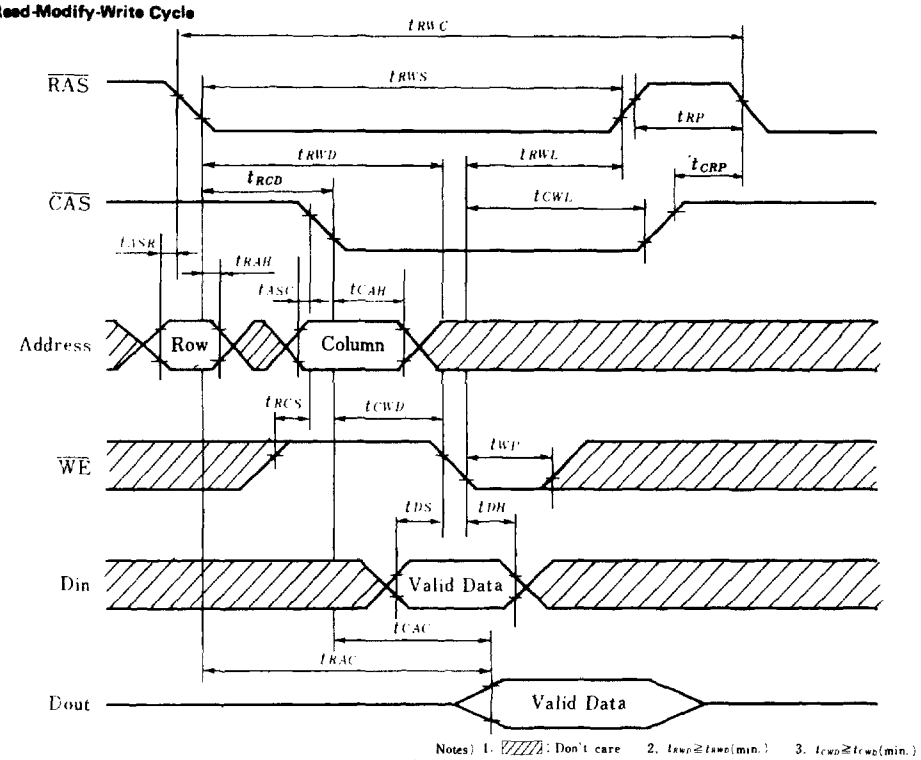


Notes) 1. ▨: Don't care
2. $t_{WCS} \geq t_{WCS}$(min.)

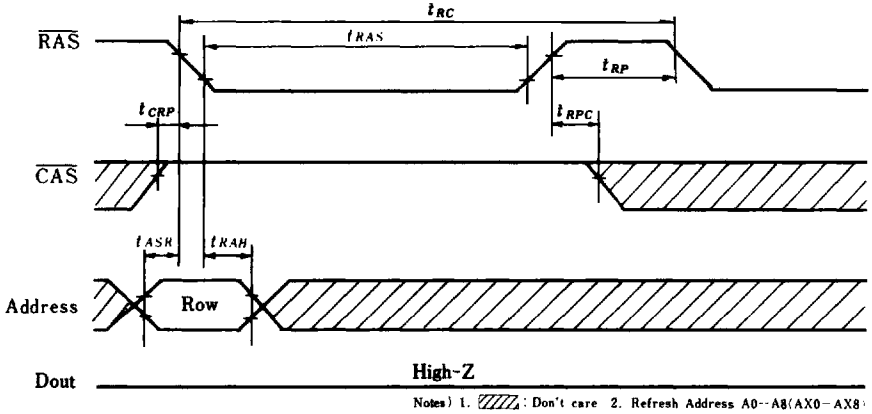
- Delayed Write Cycle



- Read-Modify-Write Cycle

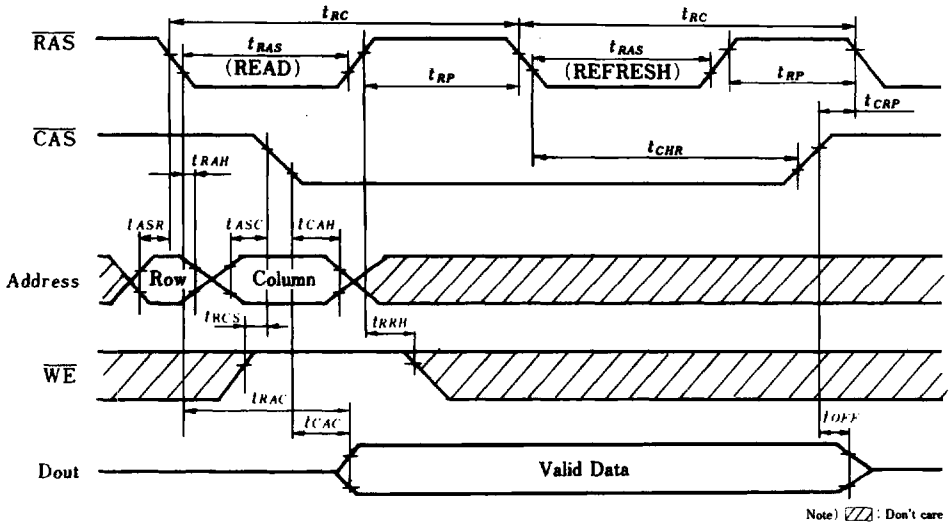


- **$\overline{RAS}$ Only Refresh Cycle**



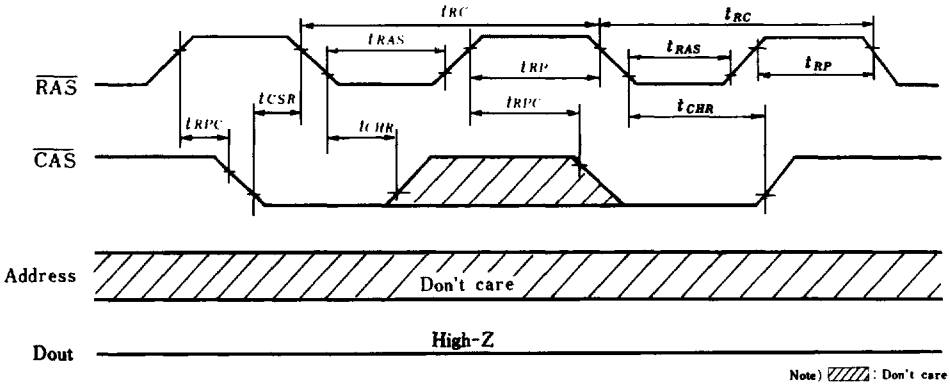
Notes) 1. ▨: Don't care 2. Refresh Address A0–A8(AX0–AX8)

- **Hidden Refresh Cycle**



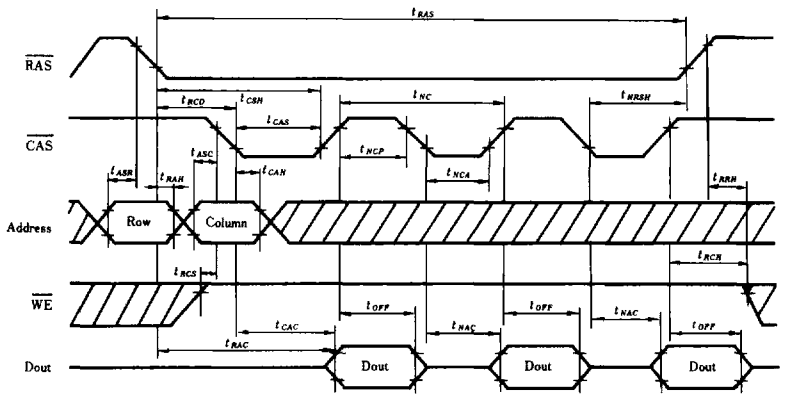
Note) ▨: Don't care

- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



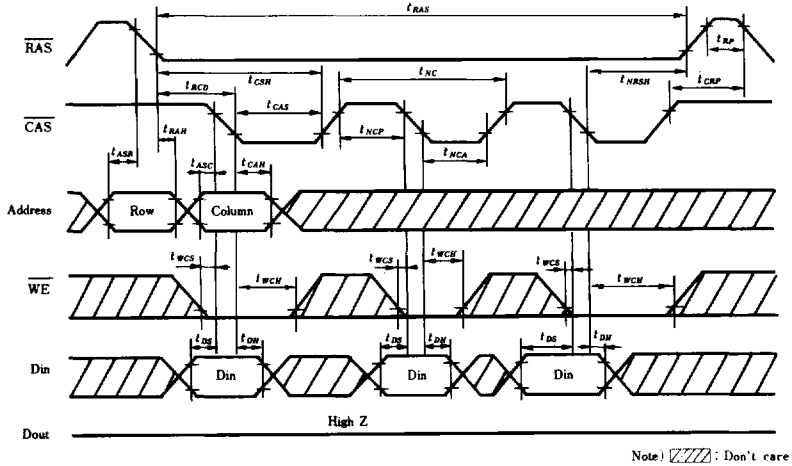
Note) ▨: Don't care

- **Nibble Mode Read Cycle**



Note) ▨ : Don't care

- **Nibble Mode Write Cycle**



Note) ▨ : Don't care

- **Nibble Mode Read Modify Write Cycle**